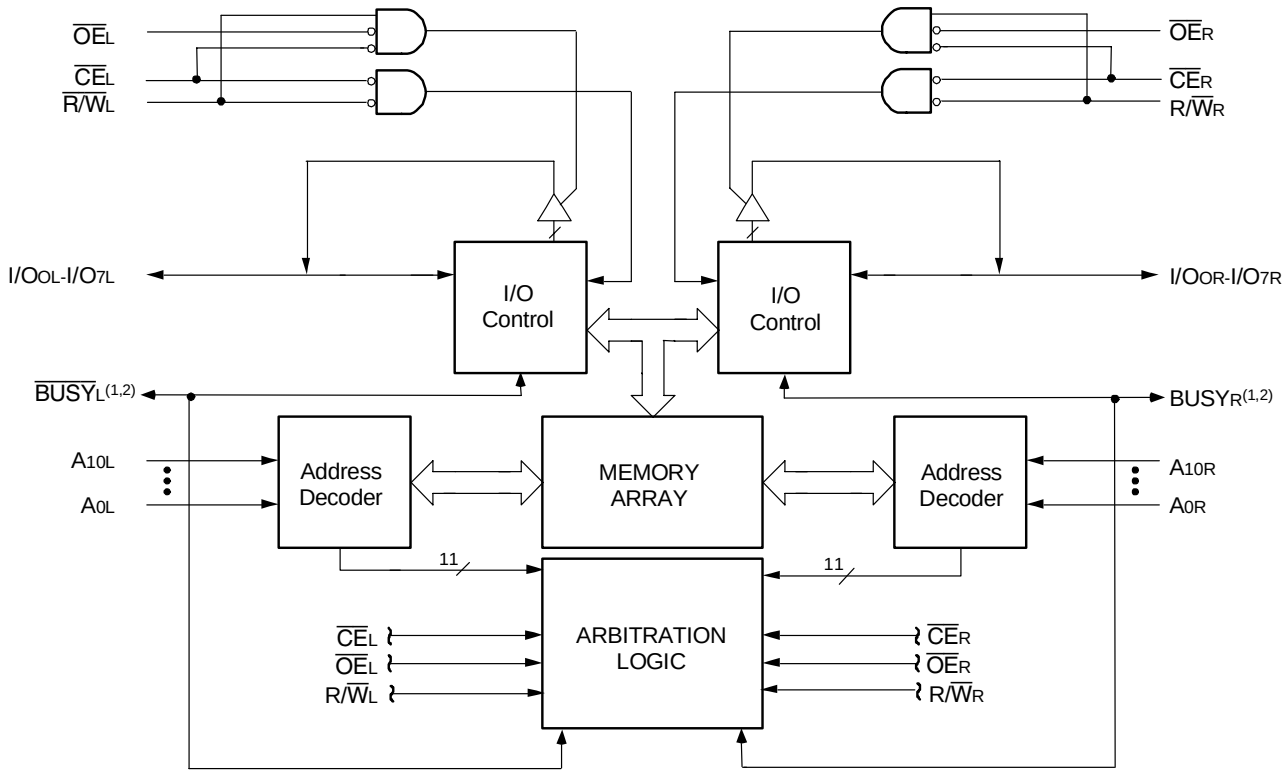
HIGH SPEED 2K x 8 DUAL PORT STATIC RAM

IDT7132SA/LA
IDT7142SA/LA

Features

- **High-speed access**
  - *Commercial: 20/25/35/55/100ns (max.)*
  - *Industrial: 25ns (max.)*
  - *Military: 25/35/55/100ns (max.)*
- **Low-power operation**
  - *IDT7132/42SA*
    Active: 325mW (typ.)
    Standby: 5mW (typ.)
  - *IDT7132/42LA*
    Active: 325mW (typ.)
    Standby: 1mW (typ.)
- **MASTER IDT7132 easily expands data bus width to 16-or-more bits using SLAVE IDT7142**
- **On-chip port arbitration logic (IDT7132 only)**
- **$\overline{BUSY}$ output flag on IDT7132; $\overline{BUSY}$ input on IDT7142**
- **Battery backup operation —2V data retention (LA only)**
- **TTL-compatible, single 5V ±10% power supply**
- **Available in 48-pin DIP, LCC and Flatpack, and 52-pin PLCC packages**
- **Military product compliant to MIL-PRF-38535 QML**
- **Industrial temperature range (–40°C to +85°C) is available for selected speeds**
- **Green parts available, see ordering information**

Functional Block Diagram



2692 drw 01

NOTES:

1. IDT7132 (MASTER): $\overline{BUSY}$ is open drain output and requires pullup resistor of 270Ω.
   IDT7142 (SLAVE): $\overline{BUSY}$ is input.
2. Open drain output: requires pullup resistor of 270Ω.

Description

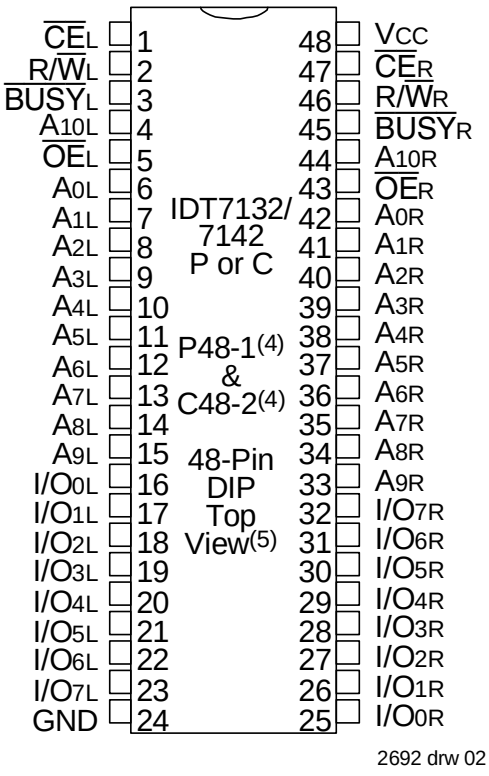
The IDT7132/IDT7142 are high-speed 2K x 8 Dual-Port Static RAMs. The IDT7132 is designed to be used as a stand-alone 8-bit Dual-Port RAM or as a "MASTER" Dual-Port RAM together with the IDT7142 "SLAVE" Dual-Port in 16-bit-or-more word width systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 16-or-more-bit memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

Both devices provide two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$ permits the on-chip circuitry of each port to enter a very low standby power mode.

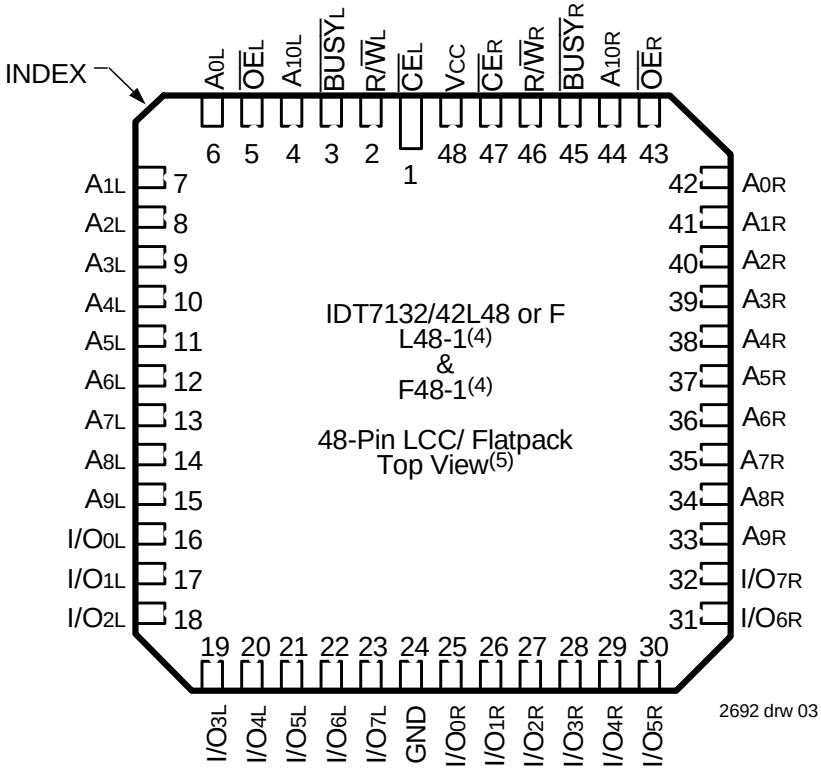
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 325mW of power. Low-power (LA) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT7132/7142 devices are packaged in a 48-pin sidebraze or plastic DIPs, 48-pin LCCs, 52-pin PLCCs, and 48-lead flatpacks. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations[1,2,3]



2692 drw 02



2692 drw 03

NOTES:
1. All V_{CC} pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. P48-1 package body is approximately .55 in x 2.43 in x .18 in.
   C48-2 package body is approximately .62 in x 2.43 in x .15 in.
   L48-1 package body is approximately .57 in x .57 in x .68 in.
   F48-1 package body is approximately .75 in x .75 in x .11 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

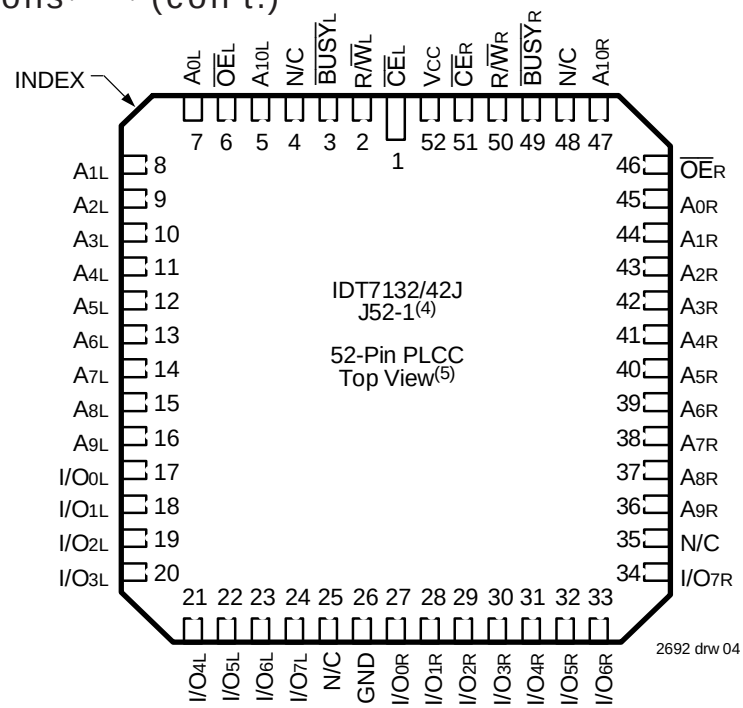
Capacitance[1] (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions[2]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 3dV	11	pF

2692 tbl 00

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dV represents the interpolated capacitance when the input and output signals switch from 3V to 0V.

Pin Configurations[1,2,3] (con't.)



NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. Package body is approximately .75 in x .75 in x .17 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Absolute Maximum Ratings[1]

Symbol	Rating	Commercial & Industrial	Military	Unit
VTERM[2]	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
TBIAS	Temperature Under Bias	-55 to +125	-65 to +135	°C
TSTG	Storage Temperature	-65 to +150	-65 to +150	°C
IOUT	DC Output Current	50	50	mA

2692 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 10%.

Recommended Operating Temperature and Supply Voltage[1,2]

Grade	Ambient Temperature	GND	Vcc
Military	-55°C to+125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%
Industrial	-40°C to +85°C	0V	5.0V ± 10%

2692 tbl 02

NOTES:
1. This is the parameter TA. This is the "instant on" case temperature.
2. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Ground	0	0	0	V
VIH	Input High Voltage	2.2	—	6.0[2]	V
VIL	Input Low Voltage	-0.5[1]	—	0.8	V

2692 tbl 03

NOTES:
1. VIL (min.) = -1.5V for pulse width less than 10ns.
2. VTERM must not exceed Vcc + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[1,5,8] (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Condition	Version		7132X20[2] 7142X20[2] Com'l Only Typ.	7132X20[2] 7142X20[2] Com'l Only Max.	7132X25[7] 7142X25[7] Com'l, Ind & Military Typ.	7132X25[7] 7142X25[7] Com'l, Ind & Military Max.	7132X35 7142X35 Com'l & Military Typ.	7132X35 7142X35 Com'l & Military Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}, Outputs Disabled f = f_{MAX}[3]	COM'L	SA	110	250	110	220	80	165	mA
				LA	110	200	110	170	80	120	
			MIL & IND	SA	—	—	110	280	80	230	
				LA	—	—	110	220	80	170	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[3]	COM'L	SA	30	65	30	65	25	65	mA
				LA	30	45	30	45	25	45	
			MIL & IND	SA	—	—	30	80	25	80	
				LA	—	—	30	60	25	60	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[6] Active Port Outputs Disabled f=f_{MAX}[3]	COM'L	SA	65	165	65	150	50	125	mA
				LA	65	125	65	115	50	90	
			MIL & IND	SA	—	—	65	160	50	150	
				LA	—	—	65	125	50	115	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[4]	COM'L	SA	1.0	15	1.0	15	1.0	15	mA
				LA	0.2	5	0.2	5	0.2	4	
			MIL & IND	SA	—	—	1.0	30	1.0	30	
				LA	—	—	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} -0.2V[6] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled f = f_{MAX}[3]	COM'L	SA	60	155	60	145	45	110	mA
				LA	60	115	60	105	45	85	
			MIL & IND	SA	—	—	60	155	45	145	
				LA	—	—	60	115	45	105	

2692 tbl 04a

Symbol	Parameter	Test Condition	Version		7132X55 7142X55 Com'l & Military Typ.	7132X55 7142X55 Com'l & Military Max.	7132X100 7142X100 Com'l & Military Typ.	7132X100 7142X100 Com'l & Military Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IL}, Outputs Disabled f = f_{MAX}[3]	COM'L	SA	65	155	65	155	mA
				LA	65	110	65	110	
			MIL & IND	SA	65	190	65	190	
				LA	65	140	65	140	
I_{SB1}	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L$ = $\overline{CE}_R$ = V_{IH}, f = f_{MAX}[3]	COM'L	SA	20	65	20	55	mA
				LA	20	35	20	35	
			MIL & IND	SA	20	65	20	65	
				LA	20	45	20	45	
I_{SB2}	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[6] Active Port Outputs Disabled f=f_{MAX}[3]	COM'L	SA	40	110	40	110	mA
				LA	40	75	40	75	
			MIL & IND	SA	40	125	40	125	
				LA	40	90	40	90	
I_{SB3}	Full Standby Current (Both Ports - All CMOS Level Inputs)	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} -0.2V V_{IN} ≥ V_{CC} -0.2V or V_{IN} ≤ 0.2V, f = 0[4]	COM'L	SA	1.0	15	1.0	15	mA
				LA	0.2	4	0.2	4	
			MIL & IND	SA	1.0	30	1.0	30	
				LA	0.2	10	0.2	10	
I_{SB4}	Full Standby Current (One Port - All CMOS Level Inputs)	$\overline{CE}_{"A"}$ ≤ 0.2V and $\overline{CE}_{"B"}$ ≥ V_{CC} -0.2V[6] V_{IN} ≥ V_{CC} - 0.2V or V_{IN} ≤ 0.2V Active Port Outputs Disabled f = f_{MAX}[3]	COM'L	SA	40	100	40	95	mA
				LA	40	70	40	70	
			MIL & IND	SA	40	110	40	110	
				LA	40	85	40	80	

2692 tbl 04b

NOTES:

1. 'X' in part numbers indicates power rating (SA or LA).
2. PLCC Package only
3. At f = f_{Max}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1/t_{RC}, and using "AC TEST CONDITIONS" of input levels of GND to 3V.
4. f = 0 means no address or control lines change. Applies only to inputs at CMOS level standby.
5. V_{CC} = 5V, T_A=+25°C for Typ and is not production tested. $V_{CC\,DC}$ = 100mA (Typ)
6. Port "A" may be either left or right port. Port "B" is opposite from port "A".
7. Not available in DIP packages.
8. Industrial temperature: for specific speeds, packages and powers contact your sales office.

DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range (V_{CC} = 5.0V ± 10%)

Symbol	Parameter	Test Conditions	7132SA 7142SA		7132LA 7142LA		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current[1]	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = 5.5V, $\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC}	—	10	—	5	µA
V_{OL}	Output Low Voltage	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OL}	Open Drain Output Low Voltage ($\overline{BUSY}$)	I_{OL} = 16mA	—	0.5	—	0.5	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

2692 tbl 05

NOTE:
1. At V_{CC} ≤ 2.0V leakages are undefined.

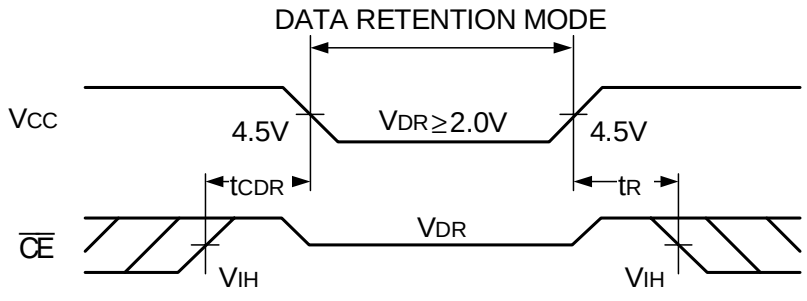
Data Retention Characteristics (LA Version Only)

Symbol	Parameter	Test Condition		Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention	V_{CC} = 2.0V		2.0	—	—	V
I_{CCDR}	Data Retention Current	$\overline{CE}$ ≥ V_{CC} -0.2V	Mil. & Ind.	—	100	4000	µA
		V_{IN} ≥ V_{CC} -0.2V or	Com'l.	—	100	1500	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time	V_{IN} ≤ 0.2V		0	—	—	ns
t_R[3]	Operation Recovery Time			t_{RC}[2]	—	—	ns

2692 tbl 06

NOTES:
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed but not production tested.

Data Retention Waveform



2692 drw 05

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range[3,5]

Symbol	Parameter	7132X20[2] 7142X20[2] Com'l Only		7132X25[2] 7142X25[2] Com'l, Ind & Military		7132X35 7142X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE								
t_{RC}	Read Cycle Time	20	—	25	—	35	—	ns
t_{AA}	Address Access Time	—	20	—	25	—	35	ns
t_{ACE}	Chip Enable Access Time	—	20	—	25	—	35	ns
t_{AOE}	Output Enable Access Time	—	11	—	12	—	20	ns
t_{OH}	Output Hold from Address Change	3	—	3	—	3	—	ns
t_{LZ}	Output Low-Z Time[1,4]	0	—	0	—	0	—	ns
t_{HZ}	Output High-Z Time[1,4]	—	10	—	10	—	15	ns
t_{PU}	Chip Enable to Power Up Time[4]	0	—	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[4]	—	20	—	25	—	35	ns

2692 tbl 08a

Symbol	Parameter	7132X55 7142X55 Com'l & Military		7132X100 7142X100 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	55	—	100	—	ns
t_{AA}	Address Access Time	—	55	—	100	ns
t_{ACE}	Chip Enable Access Time	—	55	—	100	ns
t_{AOE}	Output Enable Access Time	—	25	—	40	ns
t_{OH}	Output Hold from Address Change	3	—	10	—	ns
t_{LZ}	Output Low-Z Time[1,4]	5	—	5	—	ns
t_{HZ}	Output High-Z Time[1,4]	—	25	—	40	ns
t_{PU}	Chip Enable to Power Up Time[4]	0	—	0	—	ns
t_{PD}	Chip Disable to Power Down Time[4]	—	50	—	50	ns

2692 tbl 08b

NOTES:
1. Transition is measured 0mV from Low or High-Impedance Voltage Output Test Load (Figure 2).
2. PLCC package only.
3. 'X' in part numbers indicates power rating (SA or LA).
4. This parameter is guaranteed by device characterization, but is not production tested.
5. Industrial temperature: for specific speeds, packages and powers contact your sales office.

AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range[5,6]

Symbol	Parameter	7132X20[2] 7142X20[2] Com'l Only		7132X25[2] 7142X25[2] Com'l, Ind & Military		7132X35 7142X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time[3]	20	—	25	—	35	—	ns
t_{EW}	Chip Enable to End-of-Write	15	—	20	—	30	—	ns
t_{AW}	Address Valid to End-of-Write	15	—	20	—	30	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width[4]	15	—	15	—	25	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	10	—	12	—	15	—	ns
t_{HZ}	Output High-Z Time[1]	—	10	—	10	—	15	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1]	—	10	—	10	—	15	ns
t_{OW}	Output Active from End-of-Write[1]	0	—	0	—	0	—	ns

2692 tbl 09

Symbol	Parameter	7132X55 7142X55 Com'l & Military		7132X100 7142X100 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	
WRITE CYCLE						
t_{WC}	Write Cycle Time[3]	55	—	100	—	ns
t_{EW}	Chip Enable to End-of-Write	40	—	90	—	ns
t_{AW}	Address Valid to End-of-Write	40	—	90	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	ns
t_{WP}	Write Pulse Width[4]	30	—	55	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	20	—	40	—	ns
t_{HZ}	Output High-Z Time[1]	—	25	—	40	ns
t_{DH}	Data Hold Time	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z[1]	—	30	—	40	ns
t_{OW}	Output Active from End-of-Write[1]	0	—	0	—	ns

2692 tbl 10

NOTES:
1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2). This parameter is guaranteed by device characterization but is not production tested.
2. PLCC package only.
3. For Master/Slave combination, $t_{WC} = t_{BAA} + t_{WP}$, since R/W = V_{IL} must occur after t_{BAA}.
4. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or ($t_{WZ} + t_{DW}$) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.
5. 'X' in part numbers indicates power rating (SA or LA).
6. Industrial temperature: for specific speeds, packages and powers contact your sales office.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range(7,8)

Symbol	Parameter	7132X20(1) 7142X20(1) Com'l Only		7132X25(2) 7142X25(2) Com'l, Ind & Military		7132X35 7142X35 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Timing (For Master IDT7132 Only)								
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	20	—	20	—	20	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	20	—	20	—	20	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	20	—	20	—	20	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	20	—	20	—	20	ns
t_{WDD}	Write Pulse to Data Delay(2)	—	50	—	50	—	60	ns
t_{WH}	Write Hold After $\overline{BUSY}$(6)	12	—	15	—	20	—	ns
t_{DDD}	Write Data Valid to Read Data Delay(2)	—	35	—	35	—	35	ns
t_{APS}	Arbitration Priority Set-up Time(3)	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(4)	—	25	—	35	—	35	ns
$\overline{BUSY}$ Timing (For Slave IDT7142 Only)								
t_{WB}	Write to $\overline{BUSY}$ Input(5)	0	—	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(6)	12	—	15	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(2)	—	40	—	50	—	60	ns
t_{DDD}	Write Data Valid to Read Data Delay(2)	—	30	—	35	—	35	ns

2692 tbl 11a

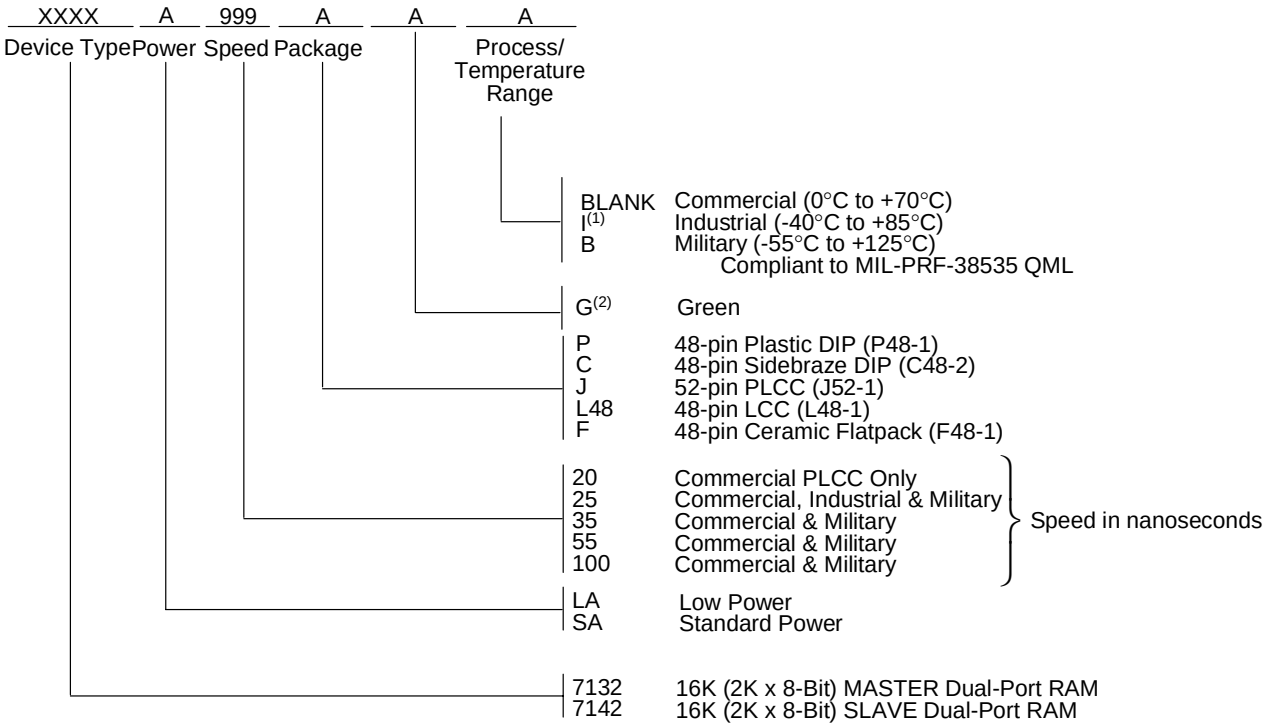
Symbol	Parameter	7132X55 7142X55 Com'l & Military		7132X100 7142X100 Com'l & Military		Unit
		Min.	Max.	Min.	Max.	
$\overline{BUSY}$ Timing (For Master IDT7132 Only)						
t_{BAA}	$\overline{BUSY}$ Access Time from Address	—	30	—	50	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address	—	30	—	50	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable	—	30	—	50	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable	—	30	—	50	ns
t_{WDD}	Write Pulse to Data Delay(2)	—	80	—	120	ns
t_{WH}	Write Hold After $\overline{BUSY}$(6)	20	—	20	—	ns
t_{DDD}	Write Data Valid to Read Data Delay(2)	—	55	—	100	ns
t_{APS}	Arbitration Priority Set-up Time(3)	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(4)	—	50	—	65	ns
$\overline{BUSY}$ Timing (For Slave IDT7142 Only)						
t_{WB}	Write to $\overline{BUSY}$ Input(5)	0	—	0	—	ns
t_{WH}	Write Hold After $\overline{BUSY}$(6)	20	—	20	—	ns
t_{WDD}	Write Pulse to Data Delay(2)	—	80	—	120	ns
t_{DDD}	Write Data Valid to Read Data Delay(2)	—	55	—	100	ns

2692 tbl 11b

NOTES:

1. PLCC package only.
2. Port-to-port delay through RAM cells from the writing port to the reading port, refer to "Timing Waveform of Write with Port -to-Port Read and BUSY."
3. To ensure that the earlier of the two ports wins.
4. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual) or $t_{DDD} - t_{DW}$ (actual).
5. To ensure that a write cycle is inhibited on port "B" during contention on port "A".
6. To ensure that a write cycle is completed on port "B" after contention on port "A".
7. 'X' in part numbers indicates power rating (SA or LA).
8. Industrial temperature: for specific speeds, packages and powers contact your sales office.

Ordering Information



2692 drw 16

NOTES:

1. Industrial temperature range is available.For specific speeds, packages and powers contact your sales office.
2. Green parts available. For specific speeds, packages and powers contact your local sales office.

Datasheet Document History

03/24/99:		Initiated datasheet document history
		Converted to new format
		Cosmetic and typographical corrections
	Pages 2 and 3	Added additional notes to pin configurations
06/08/99:		Changed drawing format
08/26/99:	Page 14	Changed Busy Logic and Width Expansion copy
11/10/99:		Replaced IDT logo
01/12/00:	Pages 1 and 2	Moved full "Description" to page 2 and adjusted page layouts
	Page 1	Added "(LAonly)" to paragraph
	Page 2	Fixed P48-1 body package description
	Page 3	Increased storage temperature parameters
		Clarified T_A parameter
	Page 4	DC Electrical parameters–changed wording from "open" to "disabled"
	Page 6	Added asteriks to Figures 1 and 3 in drw 06
	Page 14	Corrected part numbers
		Changed ±500mV to 0mV in notes
		Datasheet Document History continued on page 16